T.A.S.A
Delta Integrated Subsystems Test Review

Temple University:
Tierney Mellen, Christos Yiantos, John Do,
Colin Campbell, Lane Sandler, Nenad Markovic,
Reith Nolan, & Karla Onate

4/13/18
Presentation Outline

• Section 3: Subsystem Testing Status
• Section 4: Integrated Subsystem Testing Status
• Section 5: Plan for FMSR

• Section 8: Conclusion
3.0 Subsystem Testing Status
Subsystem Testing Status - Electrical

Front End Board:
- Data Acquisition System has been tested and data can be analyzed
- Payload SiPM array has been soldered to PCB and tested with FEB
Subsystem Testing Status - Electrical
Subsystem Testing Status - Electrical

**ADC #1**

- Entries: 178
- Mean: 424.5
- Std Dev: 460.6
Subsystem Testing Status - Electrical

Power Distribution Board

- Power system has been constructed
- Supplies sufficient power to all subsystems
- Switch mechanism needs to be tested

75%
Subsystem Testing Status - Electrical
Subsystem Testing Status - Software

Data Communication FPGA
- Active communication between the Zybo and FEB
- Writing and formatting data still in process
- GUI has been eliminated from CERN software

```c
int FEBDTP::ReadBitStream(const char *fname, UChar_t* buf) // read CITIROC SC bitstream into the buffer, buf[MAXPACKLEN]
{
    FILE *file = fopen(fname, "r");
    if(file==0) return 0;
    char line[128];
    char bits[128];
    char comment[128];
    char bit;
    int ptr, byteptr;
    int bitlen=0;
    char ascii[MAXPACKLEN];
    while (fgets(line, sizeof(line), file)) {
        bit=1; ptr=0; byteptr=0;
        printf("%d: %s",bitlen,line);
        //
        while(bit!=0x27 && bit!=0 && ptr<sizeof(line) && bitlen<MAXPACKLEN) // ASCII(0x27)= ' 
        {
            bit=line[ptr];
            ptr++;
            if(bit==0x20 || bit==0x27) continue; //ignore spaces and apostrophe
            if(Verbose) printf("%c",bit);
            ascii[bitlen]=bit;
            bitlen++;
        }
        // printf("\n");
    }
    return bitlen;
}
```
Subsystem Testing Status - Software

Enclosure sensors:
- Accelerometer, Temperature and Pressure sensors have been added
- I2C protocol is used and software is currently being written

Power Switch Mechanism:
- Tested power system functionality
Subsystem Testing Status - Mechanical

Aluminum Heat Shield: (90%)
- Tapping final lid
- In queue to CNC graphite gasket

Muon Mount: (60%)
- 3d-printed double mount
- In queue for brace plate

Deck: (50%)
- Received and built
- Need to countersink completed Heat Shields

Testing: (30%)
- Weight and Dimensional testing is continuously ongoing; not a concern
- Water tightness test, leaks should be fixed with gasket (caulk?)
- Preliminary Vibration and Heat tests by mid-April
4.0 Integrated Subsystem Testing Status
Integrated Subsystem Testing Status: Electrical

Testing Electrical and Computer Subsystems

- Proof of data storage from the Front End Board to the FPGA onto the SD card will
- Tests will be done week of April 15th
Integrated Subsystem Testing Status:
Mechanical

- Need to mount and set project components to the interior of Heat Shield
- Attach Heat Shields to Deck
- Set connections between boxes and Wallops lines
- Full system vibration test by end of April
5.0 Plan for Full Mission Simulation Review (FMSR)
Mechanical Testing

- Test for heat tolerance (Next 2 weeks)
- Dimensional Tests for weight, size and center of mass not an immediate concern, though we can check current numbers and confirm if additional weights are needed (Continuous)
- Integrate subsystems physically into payload for full system vibrational tolerance and make any necessary adjustments (End of April)
Electrical Testing

- Continue Testing FEB with SiPMs (Next 2 Weeks)
  - Testing both arrays at once
  - Dark enclosure testing
- Storing data from the FEB to the FPGA for analysis (By April 15th)
- Electrical subsystem will be tested over a full day to view particle detection at ground level
Software Testing

• Coding Tests (Next 2 Weeks)
  • Writing and saving data to SD card
  • Enclosure sensor testing
  • Encoding data for telemetry
System Level Testing

• Ground level testing rate comparison
• Full system detection testing (By April 20th)
  ○ High Altitude Testing
• Integrate subsystems physically into payload for full system vibrational tolerance and make any necessary adjustments (End of April)
Senior Design

- Final Presentation (4/23)
- Demo Day (4/27)
- Key Goals:
  - Payload physically connected and integrated
  - Muon Detector functions
  - Data read by FEB and saved by FPGA
Plan for FMSR

- Our FMSR is scheduled on 4/30
- If we meet our goals for Senior Design over the next two weeks we will be prepared for the FMSR

Major Hurdles:
- Time factor is only concern
- Data storage and formatting